ISSN: 2277-9655
Impact Factor: 1.852

IJESRT

INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH TECHNOLOGY

Simulation and Analysis of Second Generation Current Conveyor using 0.18 µm CMOS Technology

Prachi Parikh[*1], Gireeja Amin[2]

[*1] PG Student, Gujarat Technology University, Electronics and Communication, LCIT-Bhandu, Mehsana, Gujarat, India

[2]Assistant Professor. Electronics and Communication, LCIT-Bhandu, Mehsana, Gujarat, India

prachiparikh1989@gmail.com

Abstract

A wide bandwidth CMOS realization of high performance dual output second generation (CCII±) current conveyor is presented. second generation current conveyor has the advantages of a wide current and voltage bandwidths, controlled intrinsic resistances at port X, Y and Z. SPICE simulation show that the current and voltage bandwidths are respectively 2.05 GHz and 4.3 GHz for a control current of 26 µA. CCII± is a useful building block for analog circuits, especially for application requiring dual outputs. we use a translinear configuration for second generation current conveyor. The current conveyor is simulated in terms of voltage offset, current offset, current bandwidth and voltage bandwidth in 180nm CMOS technology using Mentor Graphics tools.

Keywords: Current mode circuits, Dual output current conveyor, dynamic range

Introduction

the last decade, current mode circuits have become popular. Current mode circuits exhibit reliable high frequency response, have simpler architecture, provides better dynamic ranges and operate at lower voltages than their voltage mode counterparts. Among all current mode devices, Dual output second generation Current Conveyor (CCII±) by far is the most popular one. It is widely considered as the op amp equivalent in current mode signal processing. Its performance is characterized by the voltage and current following behaviors. To exploit wideband and wide dynamic range capabilities under low power operation of current-mode signal processing, a CCII based on the translinear loop has been designed. These translinear CMOS circuits exhibit an excellent current following behavior from port X to port Z over a wide bandwidth, but the voltage following property from port Y to port X is poor and the offset voltage is rather high. In this paper, a wideband CMOS realization of the CCII based on the long tail differential pair with rail to rail input stage is designed to improve the dynamic range.

CMOS Current Conveyors

The current conveyor is a basic building block that can be implemented in analog circuit design. This was introduced by Sedra and Smith in 1968 but its real advantages and innovative impact was not clear at that time. In recent years, current-mode circuits have emerged as an important class of circuits with properties of accuracy, high frequency range and versatility in a wide range of applications. Current conveyor represents the emerging class of high performance analog circuit design based on current mode approach. It has simple architecture, wider bandwidth and capability to operate at low voltage. The current conveyors can be classified into three generations

- First Generation Current conveyor, CCI.
- Second Generation Current conveyor, CCII.
- Third Generation Current conveyor, CCIII.

In this the application of CCI± becomes difficult because both the ports X and Y have zero input impedance in order to sink currents. The port Y needs to control a current rather than to control a voltage, which is usually difficult to obtain in practical designs. This is the perhaps the greater limit of the CCI device and this reduces its flexibility and versatility.

CMOS Implementation of CCII

The second generation current conveyor (CCII) is one of the most versatile current-mode building block. For many applications, a high impedance input port is preferable in order to avoid loading effect. So, second generation current

ISSN: 2277-9655
Impact Factor: 1.852

conveyor was developed to fulfill this requirement. It has one high and one low impedance input port rather than the two low impedance input ports of CCI. The general representations of CCII± is shown in figure 1:

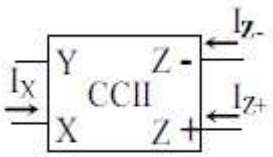

Figure1. General structures of CCII± [3]

The relation between terminal voltages and currents can be described using the following matrix:

$$\begin{bmatrix} I_Y \\ V_X \\ I_{Z\pm} \end{bmatrix} = \begin{bmatrix} 0 & a & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (1)$$

An implementation of the second generation current Conveyor using a mixed (NMOS and PMOS) translinear loop is shown in figure 2.

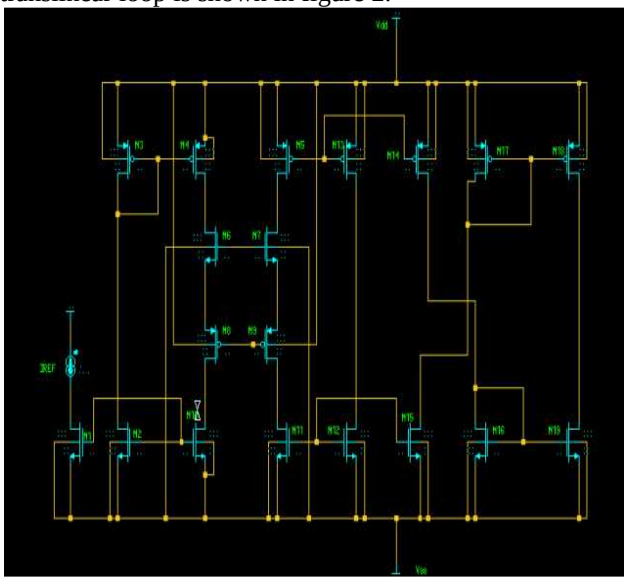

Figure2. Structures of CCII±

The mixed translinear loop formed by the transistors is characterized by the following relationship between drain currents as,

$$\sqrt{\frac{ID1}{\beta n}} + \sqrt{\frac{ID3}{\beta p}} = \sqrt{\frac{ID2}{\beta n}} + \sqrt{\frac{ID4}{\beta p}} \quad (2)$$

where βn and βp are the gain of the NMOS and PMOS transistors respectively and are given by,

$$\beta_n = \frac{\mu n Cox Wn}{2Ln} \quad (3)$$

$$\beta_p = \frac{\mu p Cox Wp}{2Lp}$$

where μn and μp are respectively the electron and holes mobility and COX is the oxide capacitance and are technology dependent.
Taking βn=βp we get,

$$2\sqrt{I_0} = \sqrt{I_{D2}} + \sqrt{I_{D4}} \quad (4)$$

The voltage gain of the circuit is given by,

$$\alpha = \frac{Vx}{Vy} = \frac{1}{1+\frac{1}{(gm2+gm4)(ro2//r04)}} \equiv 1 \quad (5)$$

From the eq. (5) it is clear that in order to maximize the voltage gain, the transconductance of the transistors M2 and M4 must be high so that the term in the denominator can be neglected. So for a given bias current I0 and length of transistor, the gm can only be increased by increasing the width of the transistors. Therefore, in order to maximize the voltage gain, the width of the transistors forming the translinear loop is kept large while designing the circuit.

Simulation Results

The simulation results are obtained in 180nm.

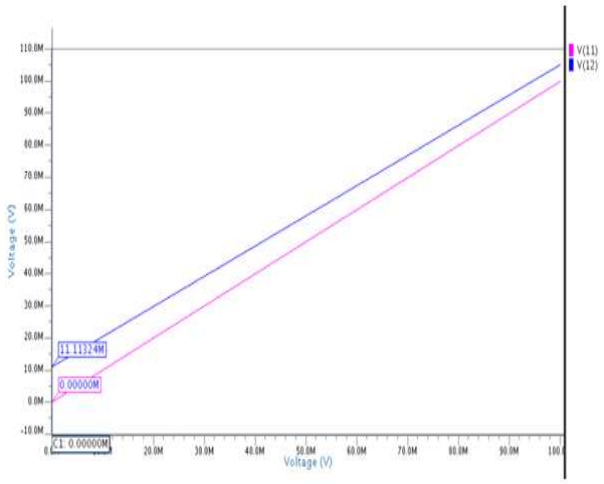

Figure3 DC voltage characteristics at port X.

ISSN: 2277-9655
Impact Factor: 1.852

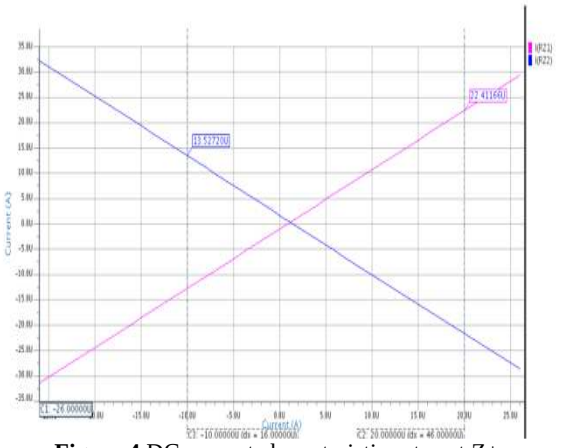

Figure 4 DC current characteristics at port Z+.

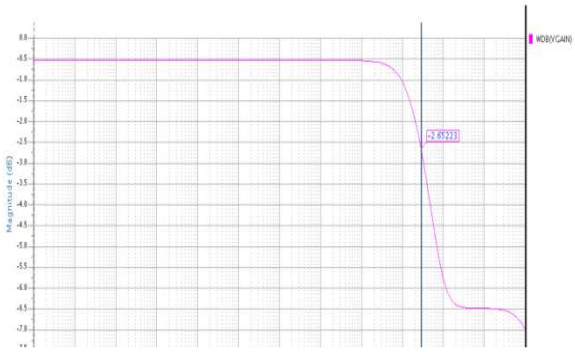

Figure 5 Frequency response of voltage gain at port X.

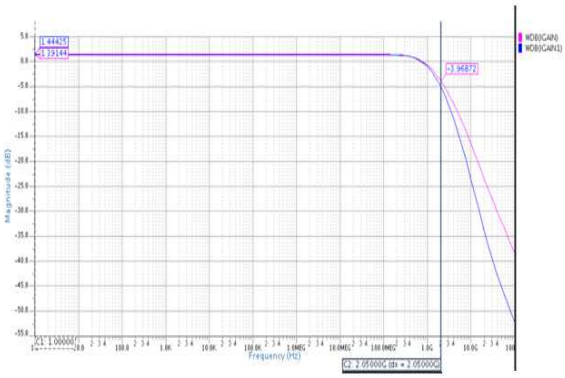

Figure 6 Frequency response of current gain and Bandwidth at ports Z+ and Z-.

Comparative Results

Table 1 Comparison of high performance CCII with different CCII proposed in [3]

PARAMETERS	CCII in [3]	CCII in Lower technology
Simulation Technology	0.35 µm	0.18 µm TSMC
Supply Voltage	±2.5V	±1.2V
Current Gain, β	1.09	1.04
Voltage Gain, α	0.96	1.03
Current B.W	1.58 GHz	2.05GHz
Voltage B.W	6.506 GHz	4.3 GHz
Output Offset Voltage	19.93mV	11.11mV
Output Offset Current	17.5µA	3.5µA
Power dissipation	-	0.59mW

From the table 1, it can be seen that high performance CCII has lower value of output offset current and voltage and also, the value of voltage and current gain of this CCII is comparable with the CCII reported in [3].

Conclusion

In this thesis, CMOS Current Conveyors for high frequency applications have been presented. current conveyor, namely, Second Generation Current Conveyor (CCII) has been analyzed and designed using TSMC 0.18µm CMOS technology process parameters. The simulation results have been presented to demonstrate the feasibility of the circuits.

The design of second generation current conveyor provides a voltage gain of 1.03 and current gain of 1.04. For a biasing current of 26µA, the circuit provides the voltage and current bandwidth of 4.3GHz and 2.05GHz respectively; hence this circuit can be used for high frequency applications. The excellent current following action is also achieved from input port to the output port.

References

[1] AmrutaBhatt, "Design and Analysis of CMOS Current Conveyor", Journal of Information, Knowledge and Research in Electronics and Communication Engineering,Nov 2012

[2] NimaAhmadpoor,SaeedMohamadzade,Most afaAhmadzadeh, "A Novel Linear Low Voltage Rail to Rail Second Generation Current Conveyor for RF Applications",Journal of Basic and Applied Scientific Research,2012.

ISSN: 2277-9655
Impact Factor: 1.852

[3] *NadhmiaBouaziz El Feki and DorraSellamiMasmoudi, "High Performance Dual-Output Second and Third Generation Current Conveyors and Current-Mode Multifunction Filter Application", Systems, Signals and Devices,6th International Multi-Conference, March 2009*

[4] *EmreArslan, AvniMorgul, "Wideband Current Conveyor with Rail to Rail Input Stage",Bogazici University Scientific Research Projects,2008*

[5] *Fei Yuan, CMOS Current-Mode Circuits for Data Communications, New York: Springer, 2007.*

[6] *Ahmed H. Madian, Soliman A. Mahmoud, Ahmed M. Soliman, "New 1.5-V CMOS second generation current conveyor based on wide range transconductor",SpringerScience,September 2006*

[7] *Shahram Minaei, Merih Yildiz Sait ,Turkoz Hakan, Kuntman,"High Swing Cmos Realization For Third Generation Current Conveyor (CCIII)", Journal Of Electrical & Electronics Engineering,2003*

[8] *Somaya I. Kayed, H. F. Ragai', M. Abou El-Ela and F. A. S. Soliman, "VLSI Design and Implementation of Analog CMOS 2nd Generation Current Conveyors", Circuits and Systems, The 2001 IEEE International Symposium Vol:4, May 2001*

[9] *Somaya I. Kayed,H. F. Ragai, M. Abou El-Ela and F. A.S. Soliman, "VLSl Design and Implementation of CMOS Current Conveyors" ,Microelectronics, 1999. ICM '99. The Eleventh International Conference, Nov. 1999*

[10] *A. Fabre, "Third- generation current conveyor: a new helpful active element", Electronics Letters vol:31, Issue:5, Mar 1995*

[11] *B. Wilson,"Recent developments in current conveyors and current-mode circuits", Circuits, Devices and Systems, IEE Proceedings G Vol:137, Issue: 2 ,Apr 1990*

[12] *Sedra,Smith,"A Second-Generation Current Conveyor and Its Applications", Proceedings of the IEEE (Vol:56 ,Issue: 8), Aug,1968*

[13] *Petri Eloranta ,Prof Chris Toumazou,"Current Conveyors".*

[14] *P. E. Allen and D. R Holberg, CMOS Analog Circuit Design, 2nd edition, Oxford University Press, 2002.*

[15] *R.J. Baker, H.W. Li, D.E. Boyce, CMOS Circuit Design Layout and Simulation, IEEE Press, 1998.*